400G QSFP-DD DR4 Specification

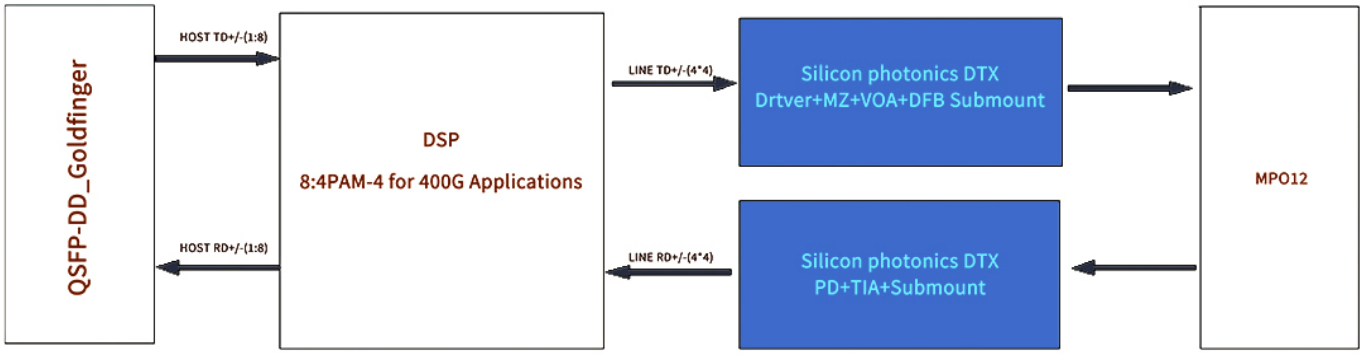
Features

- ✧ QSFP-DD Serial Optical Interface
- ◆ 8x50G PAM4 retimed 400GAUI-8 electrical interface
- ◆ MPO-12 connector with 8° angled end-face
- ◆ Up to 500m on SMF with FEC
- ✧ QSFP-DD MSA Compliant
- ◆ Hot Pluggable QSFP-DD form factor
- ◆ Compliant with CMIS5.2
- ✧ Support Protocol
- ◆ IEE802.3.bs 400GBASE-DR4 Specification compliant
- ✧ Low Power Consumption
- ◆ Less than 10.5W in temperature range of 0 to 70℃

Applications

- ◆ 400Gb/s Ethernet
- ◆ Data Center
- ◆ InfiniBand interconnects

Functional Block Diagram



1. General Description

RQDD-400G-DR4 is a Silicon Photonics 400G (4x100G) DR4 transceiver. RQDD-400G-DR4 is a fully integrated, 425 Gb/s optical transceiver for SMF links up to 500m. RQDD-400G-DR4 transmits data in compliance with the optical interface specification IEEE Std802.3-2018 Section 8 400GBASE-DR4. 400GBASE-DR4 specifies the use of 4-level pulse amplitude modulation (PAM4) at 53.125 Gbaud operating at four parallel channels with wavelength on the range of 1304.5-1317.5nm. The bit rate per lane is106.25 Gb/s, which produces an aggregate data rate of 425 Gb/s by means PSM to the transmit ports of the MPO-12 connector. The received optical lanes are paralleled from the receive MPO-12 connector ports to PIN-PD built in PIC (Photonic Integrated Circuit) to recover the PAM4 for interfacing with the electrical interface via with transimpedance amplifier (TIA) surfaced-mounted to PIC.

2. Absolute Maximum Ratings and Recommended Operating Conditions

（Table 2.1 Absolute Maximum Ratings）

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	85	°C
Case Operating Temperature	Top	0	70	
Storage Relative Humidity (non-condensation)	RH	-	85	%
Supply Voltage	Vcc	0	3.6	V
Receiver Damage Threshold, per Lane	PRdmg		5.0	dBm

（Table 2.2 Recommended Operating Conditions）

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	TC	0	70	°C
Relative Humidity (non- condensation)	RH	5	85	%
Power Supply Voltage	Vcc	-3.135	3.465	V

Supply Current	Icc		3182	mA
Total Power Consumption	PC		10.5	W
Bit Rate	BR		425	Gbps

3.Optical Specification

3.1 Optical Transmitter

（Table 3.1 Transmitter Optical Interface）

Parameter	Symbol	Min	Typical	Max	Unit
Data rate per lane	DR		53.125		GBd
Modulation format			PAM4		
Center Wavelength	λ	1304.5	1311.0	1317.5	nm
Side-mode suppression ratio	SMSR	30			dB
Average launch power, each lane	P_{AVG}	-2.9		4.0	dBm
Outer Optical Modulation Amplitude (OMA outer), each lane	P_{OMA}	-0.8		4.2	dBm
Launch power in OMA outer minus TDECQ		-2.2			dBm
Transmitter and dispersion eye closure (TDECQ), each lane	TECQ			3.4	dB
Extinction Ratio	ER	3.5			dB
Optical Return Loss Tolerance	TOL			21.4	dB/Hz
Optical Power for TX DISABLE	P_{OFF}			-15	dB

3.2 Optical Receiver

(Table 3.2 Receiver Optical Interface)

Parameter	Symbol	Min	Typical	Max	Unit
Data rate per lane	BR		53.125		GBd
Modulation format			PAM4		
Center Wavelength	λ	1304.5	1311.0	1317.5	nm

Damage threshold		THD	5			dBm
Average receive power, each lane			-5.9		4.0	dBm
Average receive power, each lane			-5.9		4.0	dBm
Receiver reflectance		Rr			-26	dB
Receiver sensitivity, each lane[1]		SEN	Max(-3.9, SECQ-5.3)			dBm
Stressed receiver sensitivity, each lane		SRS			-1.9	dBm
Rx LOS	LOS Assert		-15		-7.9	dBm
	LOS De-assert				-7.5	dBm
	LOS Hysteresis		0.5			dB

Note:

1. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

4.Electrical Specification

4.1 Electrical Specifications

(Table 4.1 Module input characteristics)

Parameter	Min	Typical	Max	Unit
Supply Voltage	3.135		3.465	V
Input Differential Impedance	90	100	110	Ω
Differential data input swing			880	mVpp
Differential data output swing			900	mVpp
Bit Error Rate			2.4E-4	
Input Logic Level High	2		Vcc	V
Input Logic Level Low	0		0.8	V
Output Logic Level High	Vcc-0.5		Vcc	V
Output Logic Level Low	0		0.4	V

(Module output characteristics at TP4)

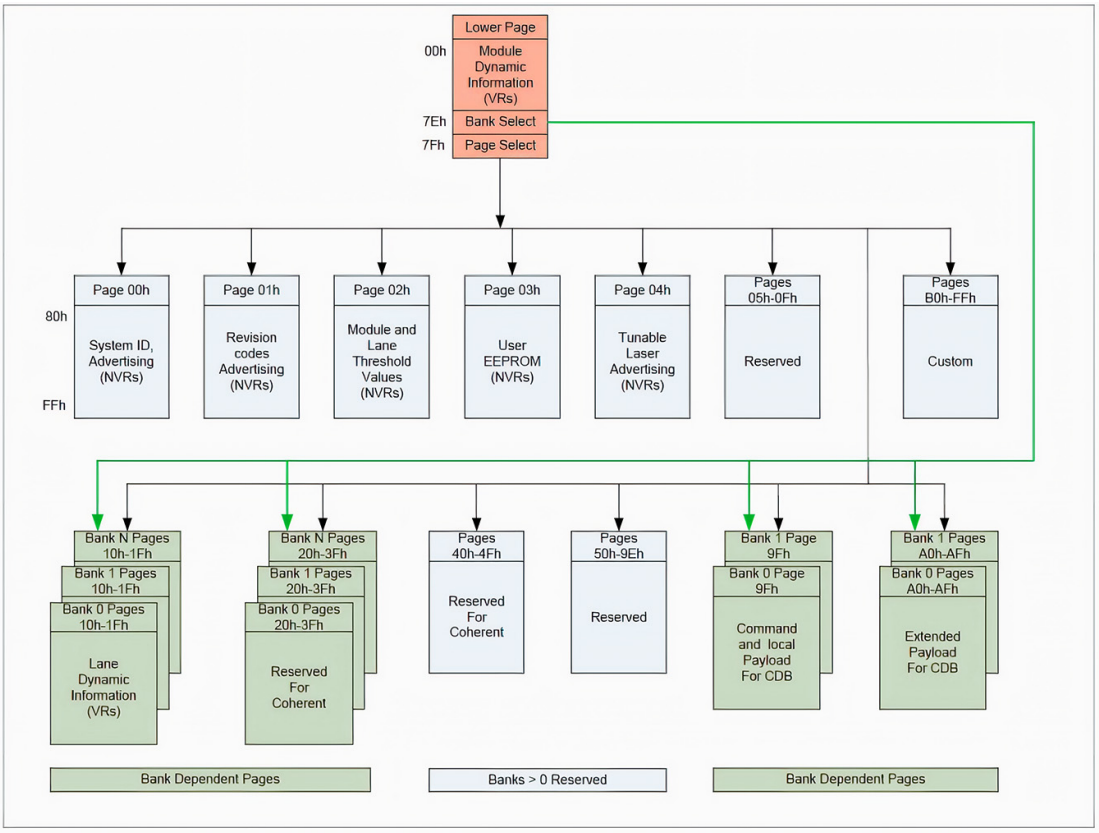
4.2 Digital Diagnostic Monitor Accuracy

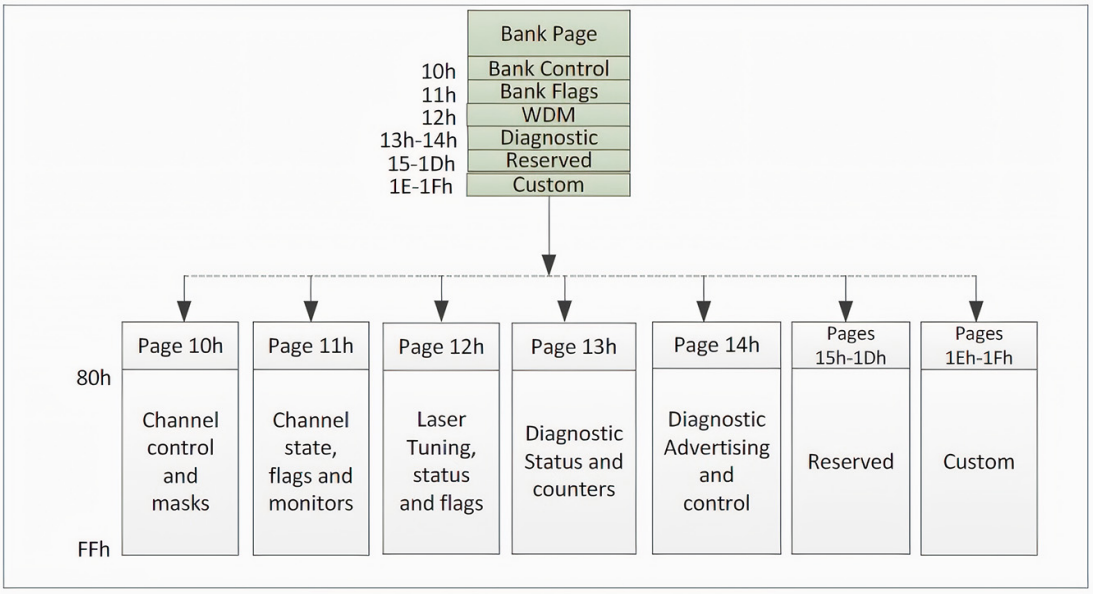
The following characteristics are defined over recommended operating conditions.

Parameter	Accuracy	Unit
Internally Measured Transceiver Temperature	+/-3	℃
Internally Measured Transceiver Supply Voltage	+/-3	%
Measured Tx Bias Current	+/-10	%
Measured Tx Output Power	+/-3	dB
Measured Rx Received Average Optical Power	+/-3	dB

5.User Interface

5.1 Management Interface

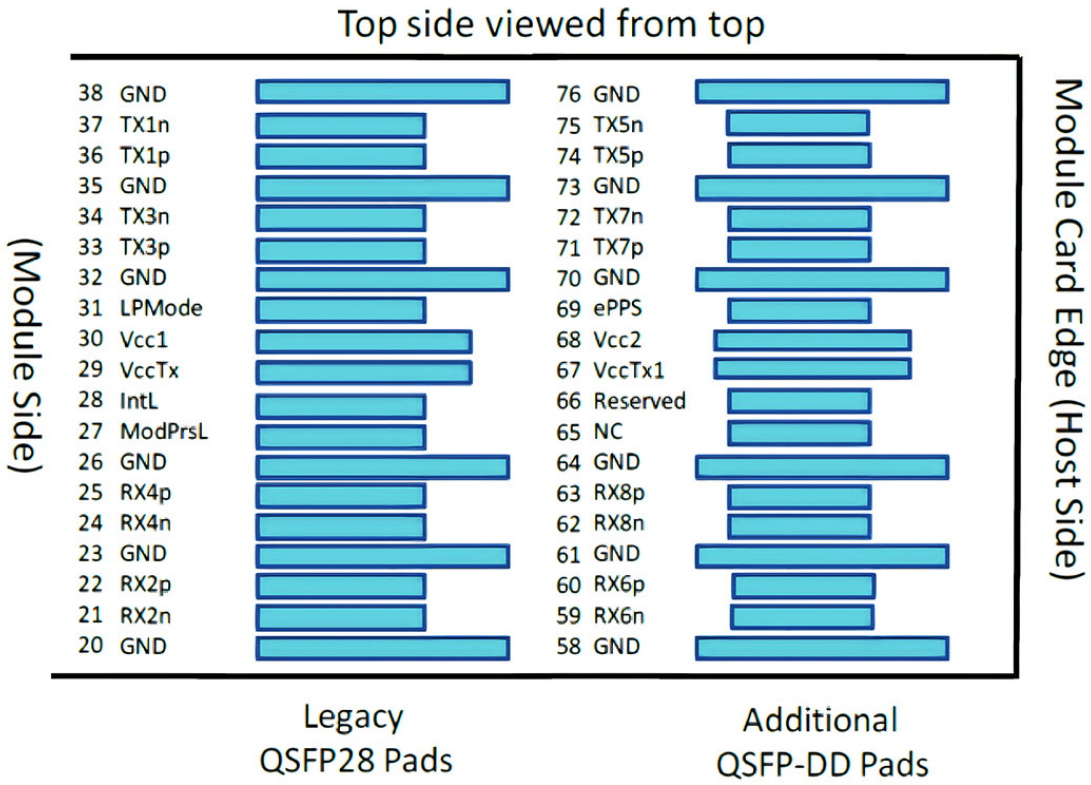




(Figure 5.1 CMIS Module Memory Map)

6. Pin Assignment and Description

QSFP-DD Transceiver Pad Layout, host PCB QSFP-DD Pinout, and PIN Descriptions are as follows:



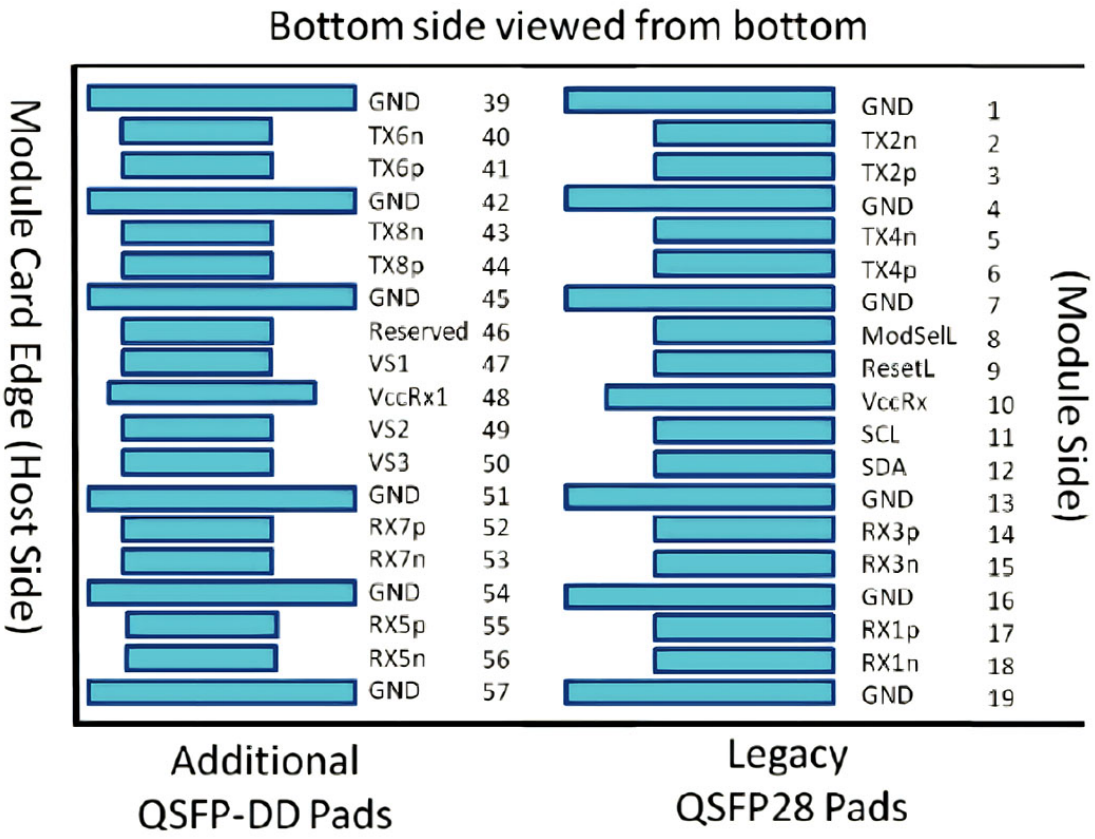


Figure 6.1 Host PCB Pinout

6.2 Pin Description

(Table 6.2 Pin Description)

Pin	Name	Logic	Description	Plug Sequence	Notes
1	Ground		GND	1B	1
2	Tx2p	CML-I	Transmitter Inverted Data Input	3B	
3	Tx2n	CML-I	Transmitter Non-Inverted Data Input	3B	
4	Ground		GND	1B	1
5	Tx4p	CML-I	Transmitter Inverted Data Input	3B	
6	Tx4n	CML-I	Transmitter Non-Inverted Data Input	3B	
7	Ground		GND	1B	1
8	ModSelL	LVTTL-I	Module Select	3B	
9	ResetL	LVTTL-I	Module Reset	3B	
10	VccRx		+3.3V Power Supply Receiver	2B	2
11	SCL	LVCMOSI/O	2-wire serial interface clock	3B	
12	SDA	LVCMOSI/O	2-wire serial interface data	3B	
13	Ground		GND	1B	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	3B	
15	Rx3n	CML-O	Receiver Inverted Data Output	3B	
16	Ground		GND	1B	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	3B	

18	Rx1n	CML-O	Receiver Inverted Data Output	3B	
19	Ground		GND	1B	1
20	Ground		GND	1B	1
21	Rx2p	CML-O	Receiver Non-Inverted Data Output	3B	
22	Rx2n	CML-O	Receiver Inverted Data Output	3B	
23	Ground		GND	1B	1
24	Rx4p	CML-O	Receiver Non-Inverted Data Output	3B	
25	Rx4n	CML-O	Receiver Inverted Data Output	3B	
26	Ground		GND	1B	1
27	ModPrsl	LVTTL-O	Module Present	3B	
28	IntL	LVTTL-O	Interrupt	3B	
29	VccTx		+3.3V Power supply transmitter	2B	2
30	Vcc1		+3.3V Power supply	2B	2
31	LPMode	LVTTL-I	Low Power mode	3B	
32	Ground		GND	1B	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	3B	
34	Tx3n	CML-I	Transmitter Inverted Data Input	3B	
35	Ground		GND	1B	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	3B	
37	Tx1n	CML-I	Transmitter Inverted Data Input	3B	
38	Ground		GND	1B	1
39	Ground		GND	1A	1
40	Tx6n	CML-I	Transmitter Inverted Data Input	3A	
41	Tx6p	CML-I	Transmitter Non-Inverted Data Output	3A	
42	Ground		GND	1A	1
43	Tx8n	CML-I	Transmitter Inverted Data Input	3A	
44	Tx8p	CML-I	Transmitter Non-Inverted Data Output	3A	
45	Ground		GND	1A	1
46	Reserved		For future use	3A	3
47	VS1		Module Vendor Specific1	3A	3
48	VccRx1		3.3V Power Supply	2A	2
49	VS2		Module Vendor Specific2	3A	3
50	VS3		Module Vendor Specific3	3A	3
51	Ground		GND	1A	1
52	Rx7p	CML-O	Receiver Non-Inverted Data Output	3A	
53	Rx7n	CML-O	Receiver Inverted Data Output	3A	
54	Ground		GND	1A	1
55	Rx5p	CML-O	Receiver Non-Inverted Data Output	3A	
56	Rx5n	CML-O	Receiver Inverted Data Output	3A	
57	Ground		GND	1A	1
58	Ground		GND	1A	1
59	Rx6n	CML-O	Receiver Inverted Data Output	3A	
60	Rx6p	CML-O	Receiver Non-Inverted Data Output	3A	

61	Ground		GND	1A	1
62	Rx8n	CML-O	Receiver Inverted Data Output	3A	
63	Rx8p	CML-O	Receiver Non-Inverted Data Output	3A	
64	Ground		GND	1A	1
65	NC		No Connect	3A	3
66	Reseved		For future use	3A	3
67	VccTx1		3.3V Power Supply	2A	2
68	VccTx1		3.3V Power Supply	2A	2
69	ePPS	LVTTL-I	Precision Time Protocol (PTP) reference clock input	3A	3
70	Ground		GND	1A	1
71	Tx7p	CML-I	Transmitter Non-Inverted Data Output	3A	
72	Tx7n	CML-I	Transmitter Inverted Data Output	3A	
73	Ground		GND	1A	1
74	Tx5p	CML-I	Transmitter Non-Inverted Data Output	3A	
75	Tx5n	CML-I	Transmitter Inverted Data Output	3A	
76	Ground		GND	1A	1

Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and reserved pads shall have an impedance to GND that is greater than 10Kohms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

7. Package Dimensions

Figure 7.1 shows the package dimensions of the module. Package dimensions are specified in QSFP-DD MSA.

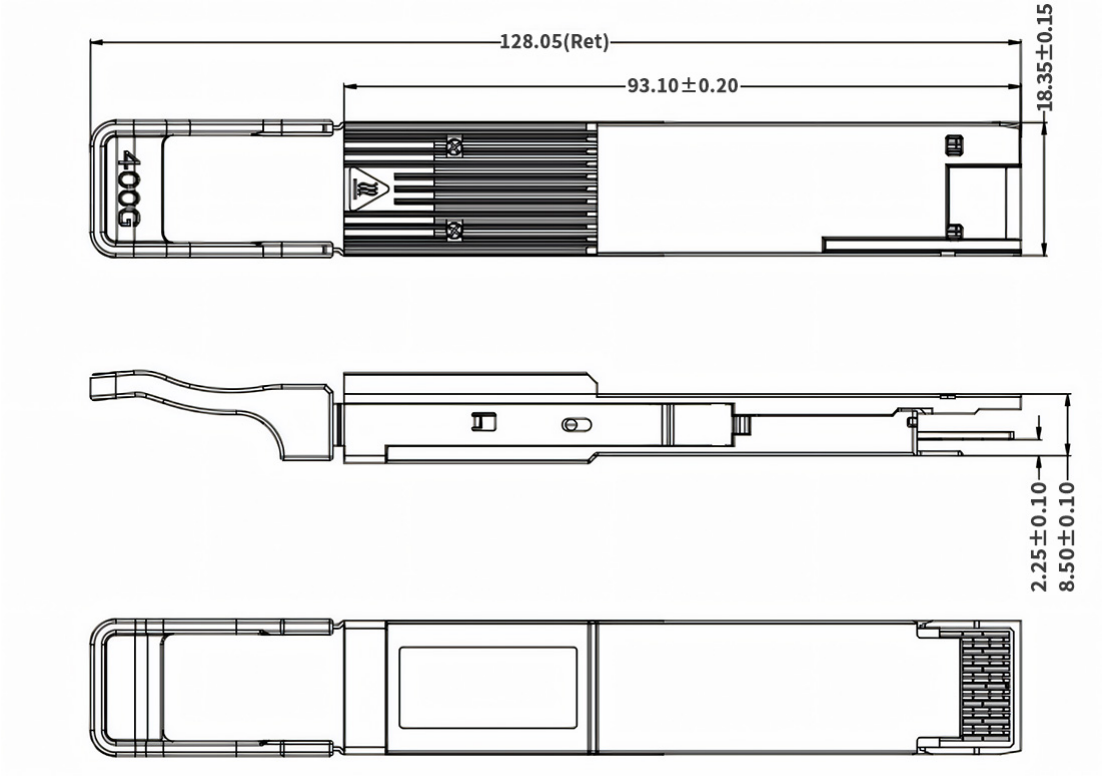


Figure 7.1 Package dimensions

9. Ordering Information

Part Number	Temperature Range	Distance	Fiber Type	E/O	O/E
RQDD-400G-DR4	0 to 70℃	500m	SMF	Siph DFB	Siph PIN